CLAIMS

What is claimed is:

1. A switch that comprises:

a plurality of front-end circuits that interface to ports through which frames are transmitted and received;

a plurality of back-end circuits that store equal-sized frame portions in stripes; and

internal links from each of the front-end circuits to each of the back-end circuits,

wherein the internal links have dynamically assigned time slots that are staggered in time between internal links from a given front-end circuit.

2. The switch of claim 1, wherein data that traverses the internal links from a front-end circuit to a back-end circuit comprises a read address.

3. The switch of claim 1, wherein data that traverses the internal links from a front-end circuit to a back-end circuit comprises a write address.

4. The switch of claim 1, wherein data that traverses the internal links from a front-end circuit to a back-end circuit comprises write data.

5. The switch of claim 1, wherein data that traverses the internal links from a back-end circuit to a front-end circuit comprises read data.

6. The switch of claim 1, wherein each of the front-end circuits includes a time slot manager configured to maintain a table of time slot allocations for frame transfers to the front-end circuit from one or more of the back-end circuits, wherein the table indicates which time slots are available for allocation, and wherein the time slot manager allocates time slots based on first-available time slots.

7. The switch of claim 6, wherein frame portions from a given port are allocated a predetermined time slot for transfer across the links to the plurality of back-end circuits.

8. The switch of claim 1, wherein a frame may be transferred from one of the plurality of back-end circuits on an unused time slot not ordinarily assigned to the frame.

9. The switch of claim 1, wherein an unused time slot is utilized by a frame waiting in a transfer queue.

10. The switch of claim 1, wherein a time slot is reassigned to fulfill a higher priority transfer.

11. The switch of claim 1, wherein each of the plurality of back-end circuits is logically divided into multiple back-end circuits.

12. The switch of claim 1, wherein data is stored on the multiple back-end circuits in a redundant fashion.

13. The switch of claim 1, wherein the time slots transfer data types selected from the group consisting of read addresses, write addresses, frame data, and a combination thereof.

14. The switch of claim 13 wherein the data types are transferred on an internal link in a defined pattern.

15. A method comprising:

receiving equal-sized portions of a frame;

storing the portions in one or more buffer lines that span multiple memory modules;

dynamically allocating to the portions a time slot on multiple internal links that couple the memory modules to an egress port; and

transferring the equal-sized portions to an egress port using a dynamically allocated time slot.

16. The method of claim 15 wherein the receiving equal-sized portions further comprises obtaining a statically assigned time slot.

17. The method of claim 15, wherein the receiving equal-sized portions further comprises sending a write address on at least one of the multiple internal links to store a portion of a frame.

18. The method of claim 15, wherein the receiving equal-sized portions further comprises converting the portion into write data.

19. The method of claim 15, wherein the transferring the equal-sized portions further comprises converting data stored in the memory modules to read data.

20. The method of claim 15, wherein the transferring the equal-sized portions further comprises sending a read address to the memory modules that a portion of a frame is desired to be read.

21. The method of claim 15, wherein said dynamically allocating includes:

maintaining at least one table of time slots on internal links;

using said at least one table to identify available time slots; and

allocating a first-available time slot from said table.

22. The method of claim 15, further comprising:

transferring the portion from an ingress port to the multiple memory modules using a predetermined time slot.

23. The method of claim 15, further comprising:

transferring the portion if the portion is in a queue from an ingress port to the multiple memory modules using a unused time slot.

24. The method of claim 15, wherein the predetermined time slot is a time slot allocated for all frames received via the ingress port.

25. The method of claim 15, wherein the allocating a first available time slot further comprises determining a priority for all frames to be transferred.

26. A Fibre Channel (FC) fabric comprising:

multiple FC switches coupled together,

wherein at least one of the FC switches is configured to receive equal-sized portions of a frame, store the portions in one or more buffer lines that span multiple memory modules, and dynamically allocate to the portions a time slot on multiple internal links that couple the memory modules to an egress port.

27. The fabric of claim 26, wherein the portions from a given port are allocated a predetermined time slot for transfer across the links to the multiple memory modules.

28. The fabric of claim 26, wherein a frame may be transferred from one of the multiple memory modules on an unused time slot not already assigned to the frame.

29. The fabric of claim 26, wherein an unused time slot is utilized by a frame waiting in a transfer queue.

30. The fabric of claim 26, wherein a time slot is reassigned to fulfill a higher priority transfer.

31. The fabric of claim 26, wherein at least one of the multiple memory modules is logically divided into multiple memory modules.

32. The fabric of claim 26, wherein data is stored on the multiple back-end circuits in a redundant fashion.

33. The fabric of claim 26, wherein the time slots transfer data types selected from the group consisting of read addresses, write addresses, frame data, and a combination thereof.

34. The fabric of claim 33, wherein the data types are transferred on an internal link in a defined pattern.

35. A network comprising:

at least two nodes; and

a Fibre Channel (FC) fabric coupling the nodes,

wherein the fabric comprises at least one switch that is configured to receive equal-sized portions of a frame, store the portions in one or more buffer lines that span multiple memory modules, and dynamically allocate to the portions a time slot on multiple internal links that couple the memory modules to an egress port.

36. The fabric of claim 35, wherein the portions from a given port are allocated a predetermined time slot for transfer across the links to the multiple memory modules.

37. The fabric of claim 35, wherein a frame may be transferred from one of the multiple memory modules on an unused time slot not already assigned to the frame.

38. The fabric of claim 35, wherein an unused time slot is utilized by a frame waiting in a transfer queue.

39. The fabric of claim 35, wherein a time slot is reassigned to fulfill a higher priority transfer.

40. The fabric of claim 35, wherein at least one of the multiple memory modules is logically divided into multiple memory modules.

41. The fabric of claim 35, wherein data is stored on the multiple back-end circuits in a redundant fashion.

42. The fabric of claim 35, wherein the time slots transfer data types selected from the group consisting of read addresses, write addresses, frame data, and a combination thereof.

43. The fabric of claim 42, wherein the data types are transferred on an internal link in a defined pattern.